An Analogue Frequency-Division Approach for Subharmonic Generation in Microwave VCOs

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Abstract- An effective and simple technique for frequency division is introduced to generate a subharmonic signal in wireless VCO circuits, thus eliminating the need for expensive digital prescalers. In this approach, frequency division is realised by injection locking an RC oscillator (multi-vibrator) at microwave frequencies. This technique is compact, efficient and MMIC compatible. The feasibility of this approach was demonstrated using a GaAs HBT RC oscillator driven by a HBT MMIC VCO operating at 4 GHz. The RC oscillator can be effectively injection locked without observable additive phase-noise degradation and generates a subharmonic clock signal at 250MHz, corresponding to a division ratio (N) of 16. The division ratio can be varied by changing the frequency of the RC oscillator. Nonlinear simulation results and analysis are also presented to explain the operating mechanism.

Introduction: As the spectrum for wireless communications extends to higher frequency bands, the problem of cost effectively phase-locking the local oscillator becomes more challenging. Digital frequency dividers for frequencies above 3 GHz are expensive; in addition, the upper operating frequency of low-cost PLL chips is also limited to approximately 3GHz. Therefore, the design of oscillator circuits with subharmonic outputs is a tenable approach when compared with the alternative solutions (e.g. divide-by-*N* IC, and frequency multiplication [1, 2]).

The conceptual block diagram of this approach is shown in Fig. 1. The oscillator output signal, f_o, is coupled to a simple analogue frequency divider that generates the frequency information for the PLL IC. The sampled signal is at a frequency f_o/N where *N* represents the division ratio. In this paper, the approach is demonstrated using an RC oscillator at 250MHz as the frequency divider with a HBT MMIC VCO operating at 4GHz corresponding to a division ratio *N* of 16.

RC oscillators have been widely used for generating clock-signals and LO synchronisation at low frequencies for more than 40 years [3], and more recently have been used in high speed clock recovery ICs in fibre-optic and wireless applications[4, 5]. However, the approach of using an injection-locked RC oscillator as a frequency divider at microwave frequencies has not been well explored. As this paper demonstrates, this approach has the advantages of high operating frequency, variable frequency-division ratio, efficient locking characteristics and low power consumption. This compares favourably with conventional analogue approaches such as regenerative dividers and harmonically locked LC oscillators [6]. Furthermore, since the circuit does not require space-consuming low frequency inductors, it is compact and MMIC compatible.

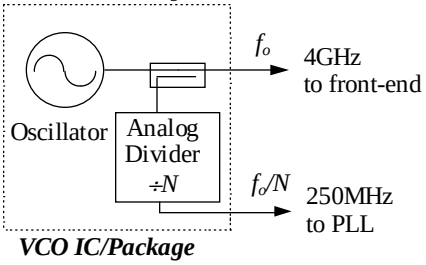

Fig. 1 Block diagram of a VCO with subharmonic output for phase locking.

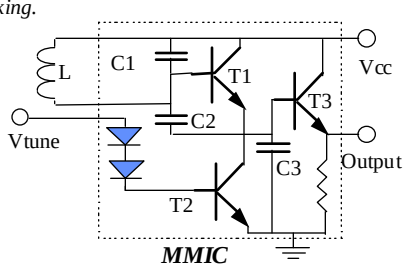

Fig. 2 The circuit schematic of the 4 GHZ MMIC VCO. The MMIC size is 0.78x0.76 mm^2.

The Circuit and Performance: The proposed approach shown in Fig. 1 was validated using a VCO and an RC oscillator circuit based on GaAs HBT technology [7]. The circuit schematic of the MMIC based VCO is shown in Fig. 2. The Colpitts oscillator is formed by T1, on-chip capacitors C1, C2, C3 and an off-chip inductor L. Frequency tuning is achieved by varying the base voltage of the active bias transistor T2. The oscillator gives +10dBm output power at 4 GHZ with a 4% tuning bandwidth.

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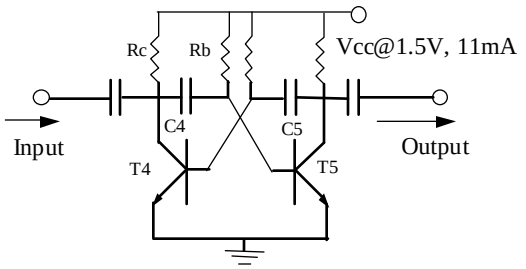


Fig. 3 The circuit schematic of the RC oscillator.

The RC oscillator circuit was fabricated using a pair of 2-finger (2x3μmx20μm) HBTs with discrete chip capacitors. The circuit schematic is shown in Fig. 3. During the oscillation process, the two HBTs T4 and T5, are alternately turned on and off by the capacitors C4 and C5 charging and discharging. A square-wave voltage signal is thus generated at the collector terminals of the transistors. The period of this alternation of on/off state is primarily determined by the relaxation between the capacitor and the input impedance of the HBT [8]. HBT devices were selected to achieve short transit time and increase the upper operating frequency of the circuit. This oscillator is designed to generate a clock signal around 250MHz, which is then injection locked by the 4 GHz VCO signal to provide the frequency division function.

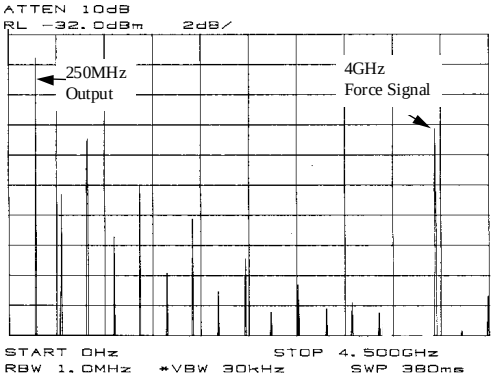


Fig. 4 The power spectrum of the output signal of the 250MHz RC oscillator under injection locking. The vertical scale of the plot is 2dB/div. The signal level was attenuated by 30dB.

The output spectrum of the RC oscillator under injection of the 4 GHz VCO signal is shown in Fig. 4. The fundamental frequency is locked at 250MHz, a factor of 1/16 of the injection frequency. The rich harmonic content of the spectrum as well as the high odd-order signals indicates a square-wave signal in the time-domain. Effective locking of the RC oscillator was achieved with a +5dBm injection signal from the VCO. Fig. 5 illustrates how the frequency divided signal tracks the injected signal as the frequency of the 4GHz VCO was varied over a frequency range of 170MHz (=16x11MHz). This corresponds to a 4% change in relative bandwidth.

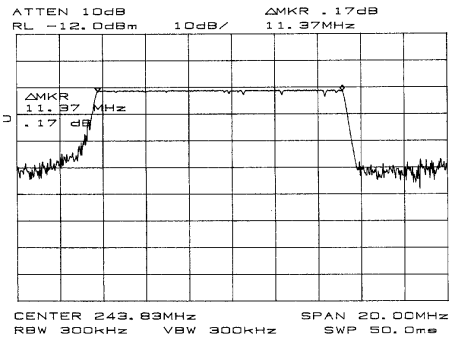
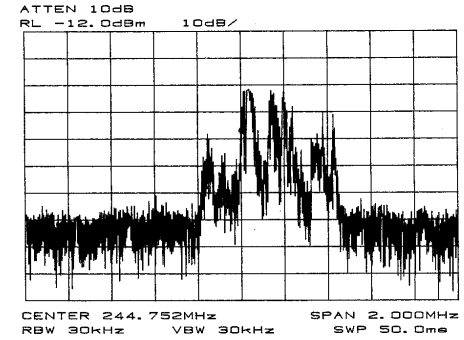
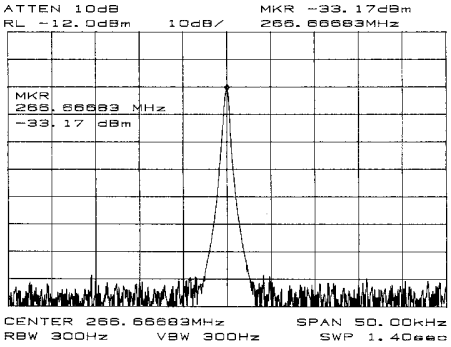


Fig. 5 The frequency trace of the RC oscillator signal tracking the frequency change in the 4 GHz VCO. The two markers indicate the locking range.



(a)



(b)

Fig. 6 The power spectra of the 250MHz clock signal, before (a) and after (b), injection of the locking signal from the 4 GHz VCO.

Low residual phase-noise is one of the most important criterion for any frequency divider to possess. The strong frequency tracking capability of the RC oscillator shown in Fig. 5 indicates its intrinsic noise will be suppressed. The frequency/phase-noise in its output signal will thus reflect the noise of the injected VCO signal [9]. Fig. 6 clearly shows the difference in spectral purity/phase-noise of the RC oscillator with and without injection locking to the stable 4GHz VCO signal. The phase-noise of the RC oscillator signal is actually lower than that of the MMIC VCO due to the frequency division process by the factor $20\log_{10}(N)$.

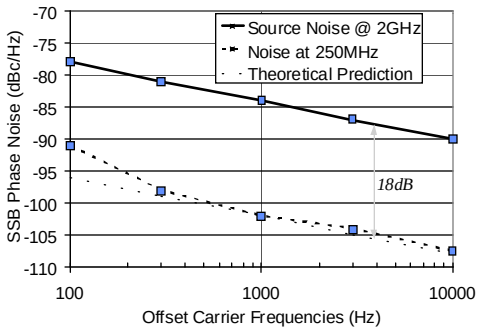


Fig. 7 The single-side-band phase noise of the RC oscillator input and output signal at 2GHz and 250MHz.

The added FM noise contribution of the frequency divider was examined by injecting a clean synthesised source into the RC oscillator and comparing the phase-noise of the input and output signals. Fig.7 shows results for an injected signal at 2GHz. The phase-noise of the 250MHz output signal is approximately 18dB lower than that of the input signal over the carrier offset frequency range, as predicted by the relationship of $20\log_{10}(N)$ for frequency division. Similar noise performance was also measured with input frequencies at 3GHz and 4GHz. The discrepancy around 100 Hz in Fig. 7 is due to the noise floor limitation of the spectrum analyser. Clearly, the results show that there is no significant signal phase-noise degradation due to the frequency divider. The absolute residual phase-noise contribution of the divider can be measured using the standard Two-port residual noise measurement method [10].

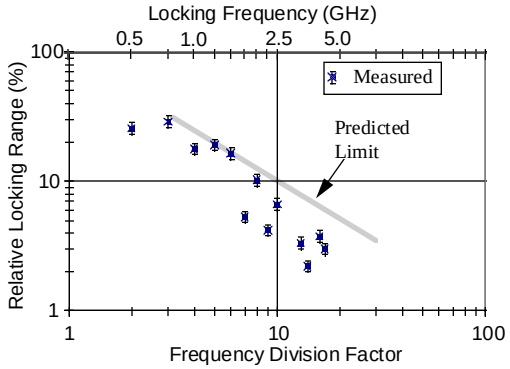


Fig. 8. The locking range of the RC oscillator as a function of the injection frequency (or the division factor).

The locking performance of the RC oscillator for other division factors was also measured by sweeping the input frequency from 500MHz (N=2) to 4.25GHz (N=17) using a synthesised source. The locking range as a function of the division factor is depicted in Fig. 8. A locking range of over 20% was recorded for N<5 which decreased to 4% for N=15..17. This frequency dependent performance is explained in the following discussion.

Discussions:

<u>*Locking of an RC Oscillator*</u>: The operation of the RC oscillator was simulated in the time-domain using a nonlinear model of the HBT [7], to provide insight into the locking mechanism. Fig. 9 shows the base voltage waveform of Transistor T5 for the RC oscillator operating in the free-running relaxation mode and when injection locked to a 900MHz signal. The simulated free-running frequency is about 240MHz, and the transition point for the HBT switching from the *off* to *on* state corresponds to a base voltage of about 1.2V. In the *off* state, the base voltage gradually increases by discharging capacitor C4: after reaching 1.2V, the HBT is turned on quickly within 100 pS. When a 900 MHz signal is injected at the input port, the base voltage is modulated by the injection signal which delays the voltage from reaching the 1.2V transition point, as shown in Fig. 9. The relaxation frequency is thus forced to slow-down to 225MHz (=900MHz/4), indicating that the RC oscillator is locked to the injection signal.

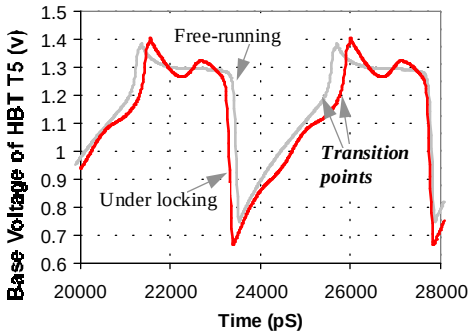


Fig. 9 The simulated waveform of the T5 base voltage with the RC oscillator operating in free-running and injection locked modes.

<u>*Frequency Dependent Locking Range:*</u> The results of Fig.9 indicate that a wider locking range can be achieved by employing higher injected signal levels. However, there is an upper limit for the locking range, Δf_{max}: the frequency change in the injection frequency (f_{inj}) has to be smaller than the natural relaxation frequency (f_{rx}) for a fixed division factor of N. This limit can be simply expressed as:

$$\frac{\Delta f_{\max}}{f_{inj}} \le \frac{f_{rx}}{f_{inj}} = \frac{1}{N} \qquad (1)$$

The locking range limit for the 250MHz RC oscillator is plotted in Fig. 8. Clearly, there is good correlation between the measured locking range and the predicted limit line for low division factors. However, above 2.5GHz (corresponding to a division ratio of 10), the two traces begin to diverge as the injection frequency approaches the switching speed of the HBT.

The HBT switching time can be approximately expressed as [11]:

$$t_S \approx \frac{\beta}{2\pi f_t} \ln\left[\frac{I_B}{I_B - 0.9\frac{I_C}{\beta}}\right] \quad (2)$$

where f_t is the cut-off frequency; β is the small signal current gain; I_B and I_C are the operating base and collector currents. The HBTs in the RC oscillator shown in Fig. 3, have a turn-on time of about 90pS with f_t of 30GHz; β of 4; I_B at 2.5mA and I_C at 11mA. For an injected sinusoidal signal to be able to affect the timing of the RC oscillator, a half cycle of the injected signal is required to be longer than the transistor switching time. The upper limit for the injection frequency can thus be estimated using the expression:

$$f_{inj} \geq \frac{1}{2 * t_s} \quad (3)$$

which corresponds to an injection frequency of 5.5 GHz for the circuit demonstrated in this paper. Clearly, this frequency can be significantly improved by increasing the HBT bias current.

Comparison of digital and analogue division approach: The primary performance characteristics of a commercial digital divider and the analogue divider are listed in Table 1. The analogue divider has the advantage of low power consumption and small die area at the expense of high input power and limited locking range; one important difference in operation is that for the digital divider, the division factor remains constant with varying input frequency. For the locked RC oscillator, however, the division ratio will vary whilst maintaining the output frequency around the natural RC resonant frequency. The natural frequency of RC oscillators is dependent upon the bias voltage, which has traditionally been considered a disadvantage since it makes the circuit bias sensitive. Conversely, this characteristic could be harnessed to make the RC oscillator a programmable controlled divider using the bias from a DAC.

Conclusions: An analogue frequency division technique to generate a subharmonic output in VCO circuits has been demonstrated by injection locking an RC oscillator. A division factor of 16 has been achieved at 4 GHz with a locking range of 170MHz and with no observable phase-noise degradation. This approach represents an attractive alternative for MMIC oscillator synchronisation and can help obviate the need to use expensive digital dividers at frequencies above 3GHz.

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Table 1 Performance comparison of digital and analogue dividers

	Device	*Frequency*	*Division Ratio*	*DC power*	*Input Power*	*Output Power*	*Chip Size*
Digital divider	MESFET	2-14GHz	8	8V, 80mA	-2dBm	-4dBm	~1mm^2
Analogue divider	GaAs HBT	0.5 - 5 GHz	2 to 16	1.5V, 11mA	5dBm	-7dBm	~0.25mm^2